CLAIMS

What is Claimed is:

1. A circuit simulation method comprising the steps of:

(a) recognizing, from mask layout data for an integrated circuit, the shape of an electronic device to be analyzed which is provided in the integrated circuit, and obtaining data concerning the size of the electronic device to be analyzed;

(b) determining the electrical characteristic of an electronic device for measurement, and measuring the size of each portion of the electronic device for measurement, as well as items each serving as an index of a stress applied to the electronic device to be analyzed;

(c) extracting, based on at least the size of each portion of the electronic device for measurement, parameters from data concerning the electrical characteristic of the electronic device for measurement which has been determined in the step (b); and

(d) utilizing a circuit simulator to select, from among the extracted parameters, a parameter suitable for each electronic device to be analyzed which is provided in the integrated circuit, and to perform circuit simulation in consideration of a stress applied to each electronic device to be analyzed.

2. The circuit simulation method of Claim 1, wherein in the step (b), at least an item serving as an index of a stress applied from an isolation insulating film to the electronic device to be analyzed is measured, and

wherein in the step (d), the circuit simulation is performed in consideration of the stress applied from the isolation insulating film to the electronic device to be analyzed.

3. The circuit simulation method of Claim 1, wherein in the step (c), a plurality of parameters are extracted for each of the equal-sized electronic devices to be analyzed, based on the items each serving as an index of a stress applied to the electronic device to be analyzed.

4. The circuit simulation method of Claim 1, wherein the method further comprises, prior to the step (d), the step of inputting an additional model to the circuit simulator, the additional model being prepared based on measurement data that has been obtained in the step (b) and that serves as an index of a stress, and

wherein in the step (d), a correction is made using the additional model when selecting a parameter suitable for each electronic device to be analyzed which is provided in the integrated circuit.

5. The circuit simulation method of Claim 1, wherein the method further comprises, prior to the step (d), the step of preparing a reference table including pieces of information for associating each electronic device to be analyzed, which is provided in the integrated circuit, with the parameter that should be assigned to the electronic device to be analyzed, and the step of inputting the reference table to the circuit simulator, the reference table being prepared based on the items each serving as an index of a stress applied to the electronic device to be analyzed, and

wherein in the step (d), the selection of the parameter suitable for each electronic device to be analyzed which is provided in the integrated circuit is automatically carried out using the reference table.

6. The circuit simulation method of Claim 5, wherein the reference table is used to

associate each electronic device to be analyzed, which is provided in the integrated circuit, with a plurality of weighted parameters.

7. The circuit simulation method of Claim 1, wherein the electronic device to be analyzed and the electronic device for measurement are each formed by a MIS transistor or a bipolar transistor.

8. The circuit simulation method of Claim 7, wherein the electronic device to be analyzed and the electronic device for measurement are each formed by a MIS transistor comprising a gate electrode, a gate insulating film, an active region and an isolation insulating film surrounding the active region, and

wherein the items, each serving as an index of a stress applied to the electronic device to be analyzed, include at least one of the position of the gate electrode in the active region, the size of the active region, and the width of the isolation insulating film.

9. The circuit simulation method of Claim 8, wherein the items, each serving as an index of a stress applied to the electronic device to be analyzed, further include at least one of the depth of the active region, a method for forming the isolation insulating film, the depth of the isolation insulating film, a material for use in forming the isolation insulating film, the size of the gate insulating film, and a material for use in forming the gate insulating film.

10. The circuit simulation method of Claim 8, wherein in the step (d), the circuit simulation is performed in consideration of a stress applied from the gate insulating film to the electronic device to be analyzed.

11. The circuit simulation method of Claim 1, wherein in the step (b), at least an item that serves as an index of a stress applied from an interlayer dielectric film to the electronic device to be analyzed is measured, and

wherein in the step (d), the circuit simulation is performed in consideration of the stress applied from the interlayer dielectric film to the electronic device to be analyzed.